ICM-40605 Datasheet

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-40605 Single-Interface MotionTracking device. The device is housed in a small 2.5x3x0.91 mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-40605 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.91 mm (14-pin LGA) package. It also features a 1K-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-40605, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports eight programmable full-scale range settings from ±15.625dps to ±2000dps, and the accelerometer supports eight programmable full-scale range settings from ±2g to ±16g.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 V to 3.6 V, and a separate digital IO supply, VDDIO from 1.71 V to 3.6 V.

The host interface can be configured to support SPI slave or I^2C slave modes. The SPI interface supports speeds up to 17 MHz and the I^2C interface supports speeds up to 1 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.91 mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- Smartphones and Tablets
- Head Mounted Displays
- Wearable Sensors

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-40605 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with programmable full-scale range of ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees/sec
- Integrated 16-bit ADC per axis
- Digitally-programmable low-pass filters
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-40605 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g*
- Integrated 16-bit ADC per axis
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The ICM-40605 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 2.5x3x0.91 mm (14-pin LGA)
- 1K byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 20,000 *g* shock tolerant
- Host interface: 17 MHz SPI / 1 MHz I^2C slave host interface
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

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3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_FS_SEL=0		±2000		º/s	2
	GYRO_FS_SEL =1		±1000		º/s	2
	GYRO_FS_SEL =2		±500		º/s	2
	GYRO_FS_SEL =3		±250		º/s	2
	GYRO_FS_SEL =4		±125		º/s	2
	GYRO_FS_SEL =5		±62.5		º/s	2
	GYRO_FS_SEL =6		±31.25		º/s	2
	GYRO_FS_SEL =7		±15.625		º/s	2
Gyroscope ADC Word Length			16		bits	2
Sensitivity Scale Factor	GYRO_FS_SEL =0		16.4		LSB/(º/s)	2
	GYRO_FS_SEL =1		32.8		LSB/(º/s)	2
	GYRO_FS_SEL =2		65.5		LSB/(º/s)	2
	GYRO_FS_SEL =3		131		LSB/(º/s)	2
	GYRO_FS_SEL =4		262		LSB/(º/s)	2
	GYRO_FS_SEL =5		524.3		LSB/(º/s)	2
	GYRO_FS_SEL =6		1048.6		LSB/(º/s)	2
	GYRO_FS_SEL =7		2097.2		LSB/(º/s)	2
Sensitivity Scale Factor Initial Tolerance	25°C	-1	±0.5	+1	%	1
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C	-0.04	±0.005	+0.04	%/ºC	3
Nonlinearity	Best fit straight line; 25°C	-0.3	±0.1	+0.3	%	3
Cross-Axis Sensitivity		-3	±1	+3	%	3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Board-level, 25°C	-10	±1	+10	º/s	3
ZRO Variation vs. Temperature	-40°C to +85°C	-0.02	±0.01	+0.02	º/s/ºC	3
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz		0.0038	0.007	º/s /√Hz	1
Total RMS Noise	Bandwidth = 100 Hz		0.038	0.07	º/s-rms	4
Gyroscope Mechanical Frequencies		25	27	29	KHz	1
Low Pass Filter Response	ODR < 1kHz	5		500	Hz	2
	ODR ≥ 1kHz	5		995	Hz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		30	40	ms	3
Output Data Rate		25		8000	Hz	2

Table 1. Gyroscope Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not guaranteed in production.
4. Calculated from Rate Noise Spectral Density.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	ACCEL_FS_SEL =0			±16		*g*	2
	ACCEL_FS_SEL =1			±8		*g*	2
	ACCEL_FS_SEL =2			±4		*g*	2
	ACCEL_FS_SEL =3			±2		*g*	2
ADC Word Length	Output in two's complement format			16		bits	2
Sensitivity Scale Factor	ACCEL_FS_SEL =0			2,048		LSB/*g*	2
	ACCEL_FS_SEL =1			4,096		LSB/*g*	2
	ACCEL_FS_SEL =2			8,192		LSB/*g*	2
	ACCEL_FS_SEL =3			16,384		LSB/*g*	2
Sensitivity Scale Factor Initial Tolerance	Component-level		-1	±0.5	+1	%	1
Sensitivity Change vs. Temperature	-40°C to +85°C		-0.025	±0.007	+0.025	%/ºC	3
Nonlinearity	Best Fit Straight Line, ±2g		-0.3	±0.1	+0.3	%	3
Cross-Axis Sensitivity			-3	±1	+3	%	3
ZERO-G OUTPUT							
Initial Tolerance	Board-level, all axes		-100	±40	+100	m*g*	3
Zero-G Level Change vs. Temperature	-40°C to +85°C	X & Y axis	-0.25	±0.15	+0.25	m*g*/ºC	3
		Z axis	-1	±0.15	+1	m*g*/ºC	3
OTHER PARAMETERS							
Power Spectral Density	@ 10 Hz			100	150	µg/√Hz	1
RMS Noise	Bandwidth = 100 Hz			1.00	1.50	mg-rms	4
Low-Pass Filter Response	ODR < 1kHz		5		500	Hz	2
	ODR ≥ 1kHz		5		995	Hz	2
Accelerometer Startup Time	From sleep mode to valid data			10	20	ms	3
Output Data Rate			25		8000	Hz	2

Table 2. Accelerometer Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not guaranteed in production.
4. Calculated from Power Spectral Density.

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3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		0.77	1	mA	2
	3-Axis Accelerometer		0.27	0.35	mA	2
	3-Axis Gyroscope		0.61	0.75	mA	2
Gyroscope Standby Mode	3-Axis Gyroscope		0.32	0.35	mA	2
Full-Chip Sleep Mode	At 25ºC		11	20	µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not guaranteed in production.

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3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		3	ms	1
Power Supply Noise			10		mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output			0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	25		8000	Hz	2
Room Temperature Offset	25°C	-5		5	°C	3
Stabilization Time				14000	µs	2
Sensitivity	Untrimmed		115.49		LSB/°C	1
Sensitivity for FIFO data			0.902		LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			1
DIGITAL INPUTS (FSYNC, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	int_tpulse_duration= 0 , 1 (100us, 8us) ;	8		100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage				0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO			V	
V_{hys}, Hysteresis			0.1		V	
V_{OL1}, LOW-Level Output Voltage 1	1 mA output current			0.2	V	
V_{OL2}, LOW-Level Output Voltage 2	50 µA output current			0.1	V	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	CLKSEL=`2b00 or gyro inactive; 25°C	-3		+3	%	1
	CLK_SEL=`2b01 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=`2b00 or gyro inactive; -40°C to +85°C			±2	%	1
	CLK_SEL=`2b01 and gyro active; -40°C to +85°C			±2	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Expected results based on design, will be updated after characterization. Not guaranteed in production.
2. Guaranteed by design.
3. Tested in production.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.26			µs	1
t_{LOW}, SCL Low Period		0.5			µs	1
t_{HIGH}, SCL High Period		0.26			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.26			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		50			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF			120	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF			120	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.5			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		0.5			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.45	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.45	µs	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

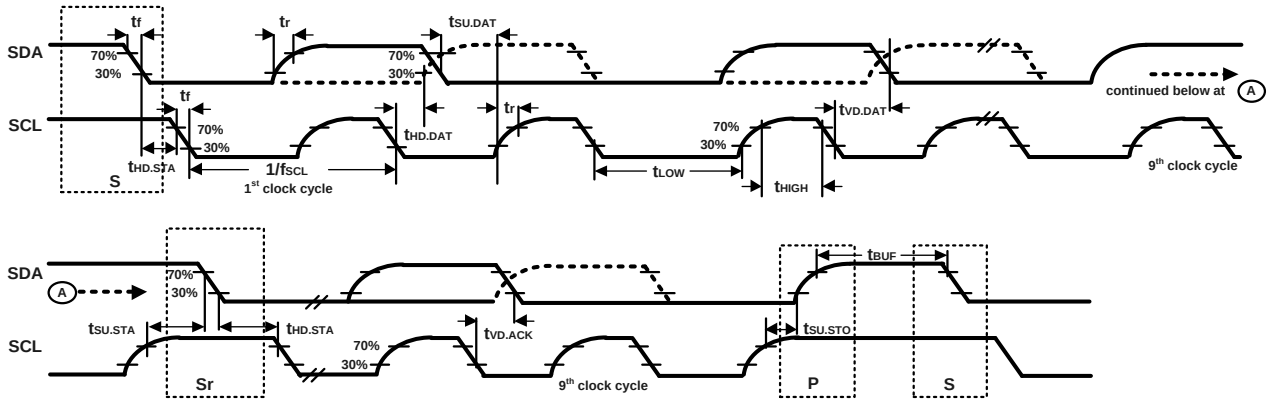

Figure 1. I²C Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

The following section is applicable to 4-wire SPI mode for the Host Interface.

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			5	MHz	1
f_{SPC}, SCLK Clock Frequency	User Adjustable (see section 11.1)			17	MHz	1
t_{LOW}, SCLK Low Period		24			ns	1
t_{HIGH}, SCLK High Period		24			ns	1
$t_{SU.CS}$, CS Setup Time		20			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDI}$, SDI Setup Time		13			ns	1
$t_{HD.SDI}$, SDI Hold Time		8			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 75 pF			24	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 75 pF	8			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				28	ns	1
t_{Fall}, SCLK Fall Time				2	ns	2
t_{Rise}, SCLK Rise Time				2	ns	2

Table 6. SPI Timing Characteristics (5 or 17-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

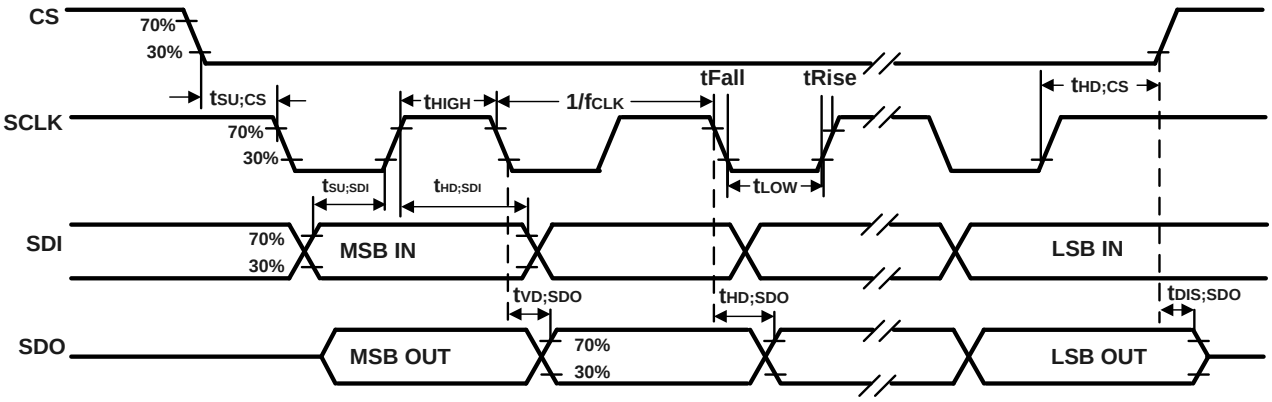

Figure 2. 4-Wire SPI Bus Timing Diagram

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3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

The following section is applicable to 3-wire SPI mode for the Host Interface.

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			5	MHz	1
f_{SPC}, SCLK Clock Frequency	User Adjustable (see section 11.1)			17	MHz	1
t_{LOW}, SCLK Low Period		24			ns	1
t_{HIGH}, SCLK High Period		24			ns	1
$t_{SU.CS}$, CS Setup Time		20			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		13			ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		8			ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 75 pF			24	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 75 pF	8			ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time				28	ns	1
t_{Fall}, SCLK Fall Time				2	ns	2
t_{Rise}, SCLK Rise Time				2	ns	2

Table 7. SPI Timing Characteristics (5 or 17-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

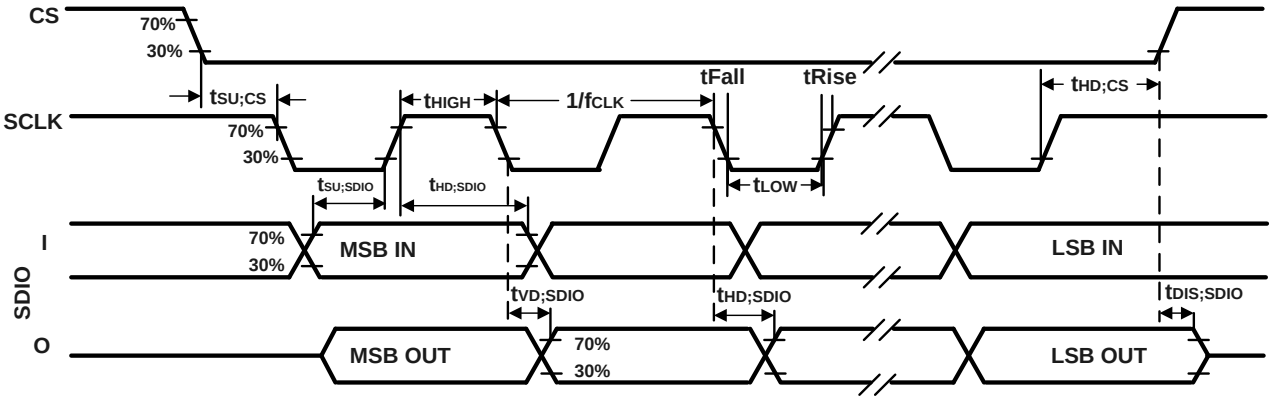

Figure 3. 3-Wire SPI Bus Timing Diagram

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3.7 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
Input Voltage Level (AD0, FSYNC, SCL, SDA)	-0.5 V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 200 V (MM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 8. Absolute Maximum Ratings

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4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

Pin Number	Pin Name	Pin Description
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I2C slave address LSB
2	RESV	No Connect or Connect to GND
3	RESV	No Connect or Connect to GND
4	INT1	Interrupt 1 (Note: INT1 is push-pull, not open drain)
5	VDDIO	IO power supply voltage
6	GND	Power supply ground
7	FSYNC	FSYNC: Frame sync input; Connect to GND if FSYNC not used
8	VDD	Power supply voltage
9	INT2	Interrupt 2 (Note: INT2 can be push-pull or open drain)
10	RESV	No Connect or Connect to GND
11	RESV	No Connect or Connect to GND
12	RESV / AP_CS	RESV: Not used, connect to VDDIO (AP I2C interface); AP_CS: AP SPI Chip select (AP SPI interface)
13	AP_SCL / AP_SCLK	AP_SCL: AP I2C serial clock; AP_SCLK: AP SPI serial clock
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I2C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)

Table 9. Signal Descriptions

Note: INT1 is a push-pull interrupt output pin. During ICM-40605 power switch on period, the INT1 status should not be logic High. There should be no external pull up resister and the host AP must ensure that INT1 pin is in INPUT mode. If this requirement is not met it may cause the ICM-40605 to become inoperable.

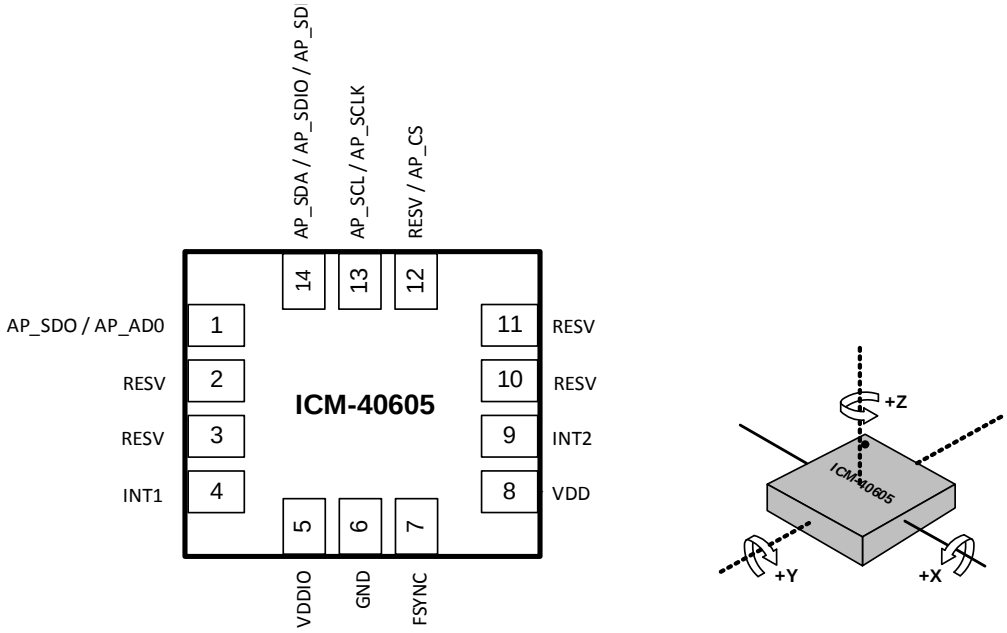

Figure 4. Pin Out Diagram for ICM-40605 2.5x3.0x0.91 mm LGA

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4.2 TYPICAL OPERATING CIRCUIT

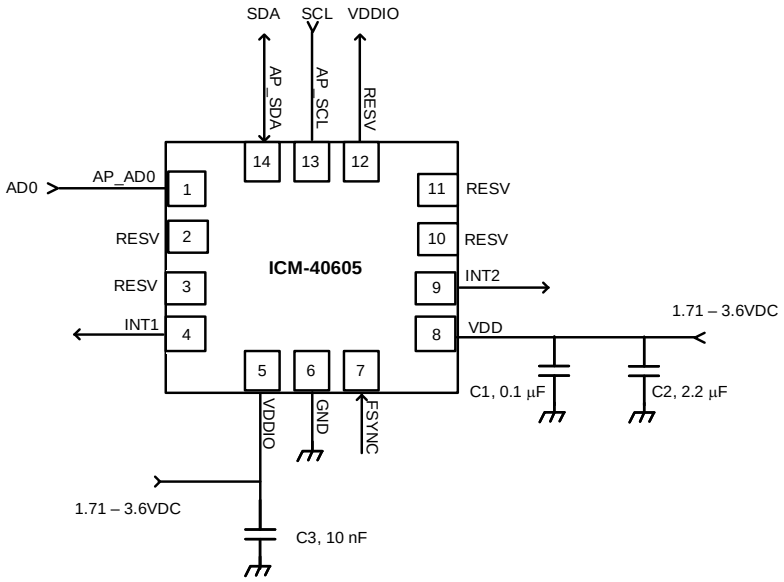

Figure 5. ICM-40605 Application Schematic (I²C Interface to Host)

Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

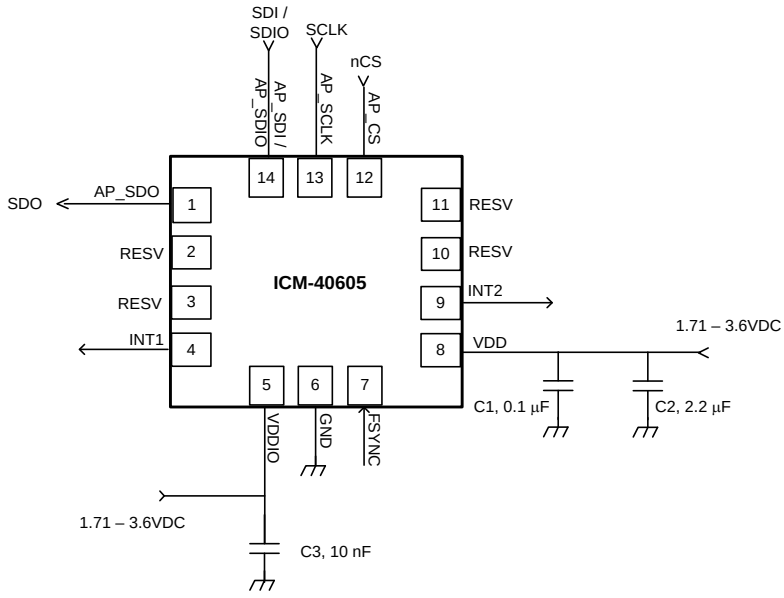

Figure 6. ICM-40605 Application Schematic (SPI 3-Wire or 4-Wire Interface to Host)

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4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
VDD Bypass Capacitors	C1 C2	X7R, 0.1µF ±10% X7R, 2.2µF ±10%	1 1
VDDIO Bypass Capacitor	C3	X7R, 10nF ±10%	1

Table 10. Bill of Materials

4.4 SYSTEM BLOCK DIAGRAM

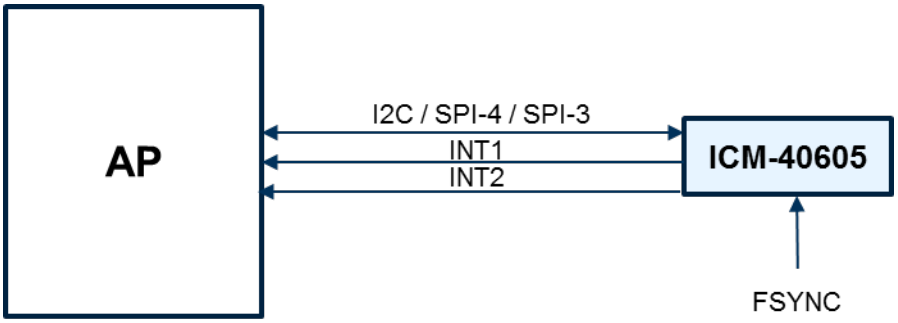

Figure 7. ICM-40605 System Block Diagram

4.5 OVERVIEW

The ICM-40605 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-40605 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 25 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-40605's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-40605's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g* and ±16*g*.

4.8 I²C AND SPI HOST INTERFACE

The ICM-40605 communicates to the application processor using either a SPI or an I²C serial interface. The ICM-40605 always acts as a slave when communicating to the application processor.

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.
When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.
The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 CLOCKING

The ICM-40605 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 FIFO

The ICM-40605 contains a 1K-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available. The ICM-40605 allows FIFO read in low-power accelerometer mode.

4.13 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.14 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-40605 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 115.49) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA * 128 / 115.49) + 25

4.15 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-40605.

4.16 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.17 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-40605.

Mode	Name	Gyro	Accel
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Noise Mode	Off	On
4	Gyroscope Low-Noise Mode	On	Off
7	6-Axis Low-Noise Mode	On	On

Table 11. Standard Power Modes for ICM-40605

5 SIGNAL PATH

The following figure shows a block diagram of the signal path in ICM-40605.

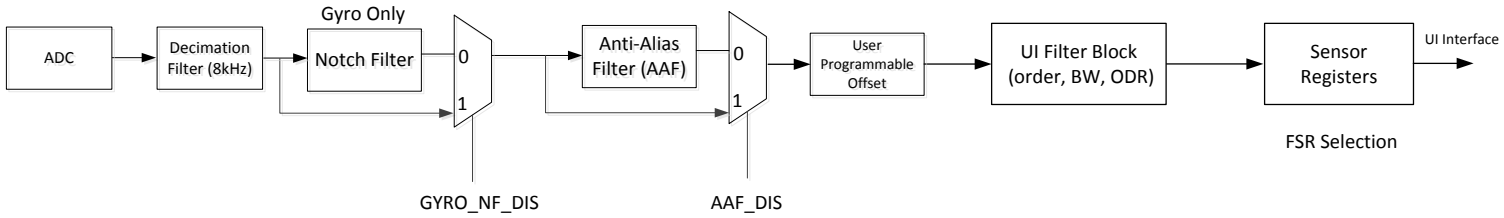

Figure 8. ICM-40605 Signal Path

The signal path starts with independent 16-bit ADCs for each axis of gyroscope and accelerometer. The ADC output goes through a Decimation Filter that has fixed bandwidth of 8kHz for ICM-40605. Other members of the ICM-406xx family may be available with other decimation filter bandwidths. Other components of the signal path are described below is further detail.

5.1 NOTCH FILTER

The Notch Filter is supported only for the gyroscope signal path. The following steps can be used to program the notch filter. Note that the notch filter is specific to each axis in the gyroscope, so the X, Y and Z axis can be programmed independently.

Frequency of Notch Filter (each axis)

To operate the Notch filter, two parameters NF_COSWZ, and NF_COSWZ_SEL must be programmed for each gyroscope axis.

Parameters NF_COSWZ are defined for each axis of the gyroscope as GYRO_X_NF_COSWZ (register bank 1, register 0x0Fh & register 0x12h), GYRO_Y_NF_COSWZ (register bank 1, register 0x10h & register 0x12h), GYRO_Z_NF_COSWZ (register bank 1, register 0x11h & register 0x12h). Note that the parameters have 9-bit values across two different registers.

Parameters NF_COSWZ_SEL are defined for each axis of the gyroscope as GYRO_X_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 3), GYRO_Y_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 4), GYRO_Z_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 5).

Each value must be calculated using the steps described below, and programmed into the corresponding register locations mentioned above.

fdesired is the desired frequency of the Notch Filter in kHz. The lower bound for fdesired is 1kHz, and the upper bound is 3kHz. Operating the notch filter outside this range is not supported.

Step1: COSWZ = cos(2*pi*fdesired/8)
Step2:
    If abs(COSWZ)≤0.875
        NF_COSWZ = round[COSWZ*256]
        NF_COSWZ_SEL = 0
    else
        NF_COSWZ_SEL = 1
        if COSWZ > 0.875
            NF_COSWZ = round [8*(1-COSWZ)*256]

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```
        else if COSWZ < -0.875
                NF_COSWZ = round [-8*(1+COSWZ)*256]
        end
End
```

Bandwidth of Notch Filter (common to all axes)

The notch filter allows the user to control the width of the notch from eight possible values using a 3-bit parameter GYRO_NF_BW_SEL in register bank 1, register 0x13h, bits 6:4. This parameter is common to all three axes.

GYRO_NF_BW_SEL	Notch Filter Bandwidth (Hz)
0	362
1	170
2	83
3	41
4	21
5	11
6	5
7	3

The notch filter can be selected or bypassed by using the parameter GYRO_NF_DIS in register bank 1, register 0x0Bh, bit 0 as shown below.

GYRO_NF_DIS	Function
0	Enable notch filter
1	Disable notch filter

5.2 ANTI-ALIAS FILTER

Anti-alias filters for gyroscope and accelerometer can be independently programmed to have bandwidths ranging from 10 Hz to 995 Hz. To program the anti-alias filter for a required bandwidth, use the table below to map the bandwidth to register values as shown:

a. Register bank 2, register 0x03h, bits 6:1, ACCEL_AAF_DELT: Code from 1 to 63 that allows programming the bandwidth for accelerometer anti-alias filter
b. Register bank 2, register 0x04h, bits 7:0 and Bank 2, register 0x05h, bits 3:0, ACCEL_AAF_DELTSQR: Square of the delt value for accelerometer
c. Register bank 2, register 0x05h, bits 7:4, ACCEL_AAF_BITSHIFT: Bitshift value for accelerometer used in hardware implementation
d. Register bank 1, register 0x0Ch, bits 5:0, GYRO_AAF_DELT: Code from 1 to 63 that allows programming the bandwidth for gyroscope anti-alias filter
e. Register bank 1, register 0x0Dh, bits 7:0 and Bank 1, register 0x0Eh, bits 3:0, GYRO_AAF_DELTSQR: Square of the delt value for gyroscope
f. Register bank 1, register 0x0Eh, bits 7:4, GYRO_AAF_BITSHIFT: Bitshift value for gyroscope used in hardware implementation

3dB Bandwidth (Hz)	ACCEL_AAF_DELT; GYRO_AAF_DELT	ACCEL_AAF_DELTSQR; GYRO_AAF_DELTSQR	ACCEL_AAF_BITSHIFT; GYRO_AAF_BITSHIFT
10	1	1	15
21	2	4	13

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32	3	9	12
42	4	16	11
53	5	25	10
64	6	36	10
76	7	49	9
87	8	64	9
99	9	81	9
110	10	100	8
122	11	121	8
134	12	144	8
146	13	169	8
158	14	196	7
171	15	225	7
184	16	256	7
196	17	289	7
209	18	324	7
222	19	361	6
236	20	400	6
249	21	441	6
263	22	484	6
277	23	529	6
291	24	576	6
305	25	625	6
319	26	676	6
334	27	729	5
349	28	784	5
364	29	841	5
379	30	900	5
394	31	961	5
410	32	1024	5
425	33	1089	5
441	34	1156	5
458	35	1225	5
474	36	1296	5
490	37	1369	4
507	38	1444	4
524	39	1521	4
541	40	1600	4
559	41	1681	4
576	42	1764	4
594	43	1849	4
612	44	1936	4
631	45	2025	4
649	46	2116	4

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668	47	2209	4
687	48	2304	4
706	49	2401	4
725	50	2500	4
745	51	2601	4
764	52	2704	4
784	53	2809	3
804	54	2916	3
825	55	3025	3
845	56	3136	3
866	57	3249	3
887	58	3364	3
908	59	3481	3
930	60	3600	3
951	61	3721	3
973	62	3844	3
995	63	3969	3

The anti-alias filter can be selected or bypassed for the gyroscope by using the parameter GYRO_AAF_DIS in register bank 1, register 0x0Bh, bit 1 as shown below.

GYRO_AAF_DIS	Function
0	Enable gyroscope anti-aliasing filter
1	Disable gyroscope anti-aliasing filter

The anti-alias filter can be selected or bypassed for the accelerometer by using the parameter ACCEL_AAF_DIS in register bank 2, register 0x03h, bit 0 as shown below.

ACCEL_AAF_DIS	Function
0	Enable accelerometer anti-aliasing filter
1	Disable accelerometer anti-aliasing filter

5.3 USER PROGRAMMABLE OFFSET

Gyroscope and accelerometer offsets can be programmed by the user by using registers OFFSET_USER0, through OFFSET_USER8, in bank 0, registers 0x77h through 0x7Fh as shown below.

Register Address	Register Name	Bits	Function
0x77h	OFFSET_USER0	7:0	Lower bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x78h	OFFSET_USER1	3:0	Upper bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
		7:4	Upper bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x79h	OFFSET_USER2	7:0	Lower bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

0x7Ah	OFFSET_USER3	7:0	Lower bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x7Bh	OFFSET_USER4	3:0	Upper bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
		7:4	Upper bits of X-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Ch	OFFSET_USER5	7:0	Lower bits of X-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Dh	OFFSET_USER6	7:0	Lower bits of Y-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Eh	OFFSET_USER7	3:0	Upper bits of Y-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
		7:4	Upper bits of Z-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Fh	OFFSET_USER8	7:0	Lower bits of Z-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.

5.4 UI FILTER BLOCK

The UI filter block can be programmed to select filter order and bandwidth independently for gyroscope and accelerometer.

Gyroscope filter order can be selected by programming the parameter GYRO_UI_FILT_ORD in register bank 0, register 0x51h, bits 3:2, as shown below.

GYRO_UI_FILT_ORD	Filter Order
00	1st order
01	2nd order
10	3rd order
11	Reserved

Accelerometer filter order can be selected by programming the parameter ACCEL_UI_FILT_ORD in register bank 0, register 0x53h, bits 4:3, as shown below.

ACCEL_UI_FILT_ORD	Filter Order
00	1st order
01	2nd order
10	3rd order
11	Reserved

Gyroscope and accelerometer filter 3dB bandwidth can be selected by programming the parameter GYRO_UI_FILT_BW in register bank 0, register 0x52h, bits 3:0, and the parameter ACCEL_UI_FILT_BW in register bank 0, register 0x52h, bits 7:4, as shown below. The values shown in bold correspond to low power and the values shown in italics correspond to low latency. User can select the appropriate setting based on the application requirements for power and latency.

3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD = 0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW							
GYRO/ACCEL_ODR	**ODR(Hz)**	0	1	2	3	4	5	6	7
3	8000	*2096.30*							

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4	4000	*1048.10*							
5	2000	*524.00*							
6	1000	**498.30**	**184.10**	**158.70**	**111.00**	**92.40**	**59.60**	**48.80**	**25.30**
7	200	**99.60**	**73.70**	**63.50**	**44.40**	**37.00**	**23.80**	**19.50**	**10.10**
8	100	**49.80**	*73.70*	*63.50*	**44.40**	**37.00**	**23.80**	**19.50**	**10.10**
9	50	**24.90**	*73.70*	*63.50*	*44.40*	*37.00*	**23.80**	**19.50**	**10.10**
10	25	**12.50**	*73.70*	*63.50*	*44.40*	*37.00*	*23.80*	*19.50*	**10.10**

The corresponding group delay values are in the following table.

Group Delay (ms) for GYRO/ACCEL_UI_FILT_ORD = 0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW							
GYRO/ACCEL_ODR	**ODR(Hz)**	0	1	2	3	4	5	6	7
3	8000	*0.33*							
4	4000	*0.52*							
5	2000	*0.89*							
6	1000	**0.67**	**2.14**	**2.33**	**2.85**	**3.17**	**4.19**	**4.79**	**7.87**
7	200	**2.76**	**5.14**	**5.60**	**6.90**	**7.71**	**10.24**	**11.77**	**19.45**
8	100	**5.37**	*5.14*	*5.60*	**6.90**	**7.71**	**10.24**	**11.77**	**19.45**
9	50	**10.60**	*5.14*	*5.60*	*6.90*	*7.71*	**10.24**	**11.77**	**19.45**
10	25	**21.05**	*5.14*	*5.60*	*6.90*	*7.71*	*10.24*	*11.77*	**19.45**

3dB Bandwidth and Group Delay values are shown for 2nd order and 3rd order filters in the tables below.

3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD = 1 (2nd order filter)									
		GYRO/ACCEL_UI_FILT_BW							
GYRO/ACCEL_ODR	**ODR(Hz)**	0	1	2	3	4	5	6	7
3	8000	*2096.30*							
4	4000	*1048.10*							
5	2000	*524.00*							
6	1000	**493.30**	**204.90**	**173.60**	**117.50**	**97.10**	**59.60**	**48.00**	**26.80**
7	200	**98.70**	**82.00**	**69.40**	**47.00**	**38.80**	**23.80**	**19.20**	**10.70**
8	100	**49.30**	*82.00*	*69.40*	**47.00**	**38.80**	**23.80**	**19.20**	**10.70**
9	50	**24.70**	*82.00*	*69.40*	*47.00*	*38.80*	**23.80**	**19.20**	**10.70**
10	25	**12.30**	*82.00*	*69.40*	*47.00*	*38.80*	*23.80*	*19.20*	**10.70**

Group Delay (ms) for GYRO/ACCEL_UI_FILT_ORD = 1 (2nd order filter)									
		GYRO/ACCEL_UI_FILT_BW							
GYRO/ACCEL_ODR	**ODR(Hz)**	0	1	2	3	4	5	6	7
3	8000	*0.33*							
4	4000	*0.52*							
5	2000	*0.89*							
6	1000	**0.79**	**2.35**	**2.61**	**3.34**	**3.78**	**5.30**	**6.23**	**9.96**
7	200	**3.36**	**5.65**	**6.31**	**8.13**	**9.23**	**13.04**	**15.37**	**24.68**
8	100	**6.57**	*5.65*	*6.31*	**8.13**	**9.23**	**13.04**	**15.37**	**24.68**
9	50	**12.99**	*5.65*	*6.31*	*8.13*	*9.23*	**13.04**	**15.37**	**24.68**

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10	25	**25.84**	*5.65*	*6.31*	*8.13*	*9.23*	*13.04*	*15.37*	**24.68**

3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD = 2 (3rd order filter)									
		GYRO/ACCEL_UI_FILT_BW							
GYRO/ACCEL_ODR	**ODR(Hz)**	0	1	2	3	4	5	6	7
3	8000	*2096.30*							
4	4000	*1048.10*							
5	2000	*524.00*							
6	1000	**492.90**	**215.60**	**179.40**	**118.90**	**97.90**	**60.80**	**50.30**	**18.80**
7	200	**98.60**	**86.30**	**71.70**	**47.60**	**39.20**	**24.30**	**20.10**	**7.50**
8	100	**49.30**	*86.30*	*71.70*	**47.60**	**39.20**	**24.30**	**20.10**	**7.50**
9	50	**24.60**	*86.30*	*71.70*	*47.60*	*39.20*	**24.30**	**20.10**	**7.50**
10	25	**12.30**	*86.30*	*71.70*	*47.60*	*39.20*	*24.30*	*20.10*	**7.50**

Group Delay (ms) for GYRO/ACCEL_UI_FILT_ORD = 2 (3rd order filter)									
		GYRO/ACCEL_UI_FILT_BW							
GYRO/ACCEL_ODR	**ODR(Hz)**	0	1	2	3	4	5	6	7
3	8000	*0.33*							
4	4000	*0.52*							
5	2000	*0.89*							
6	1000	**0.94**	**2.64**	**3.02**	**4.06**	**4.69**	**6.74**	**7.88**	**17.35**
7	200	**4.11**	**6.38**	**7.34**	**9.94**	**11.52**	**16.64**	**19.48**	**43.15**
8	100	**8.08**	*6.38*	*7.34*	**9.94**	**11.52**	**16.64**	**19.48**	**43.15**
9	50	**16.02**	*6.38*	*7.34*	*9.94*	*11.52*	**16.64**	**19.48**	**43.15**
10	25	**31.89**	*6.38*	*7.34*	*9.94*	*11.52*	*16.64*	*19.48*	**43.15**

5.5 ODR AND FSR SELECTION

Gyroscope ODR can be selected by programming the parameter GYRO_ODR in bank 0, register 0x4Fh, bits 3:0 as shown below.

GYRO_ODR	Gyroscope ODR Value
0000	Reserved
0001	Reserved
0010	Reserved
0011	8kHz
0100	4kHz
0101	2kHz
0110	1kHz
0111	200Hz (default)
1000	100Hz
1001	50Hz
1010	25Hz
1011	Reserved
1100	Reserved

1101	Reserved
1110	Reserved
1111	Reserved

Gyroscope FSR can be selected by programming the parameter GYRO_FS_SEL in bank 0, register 0x4Fh, bits 7:5 as shown below.

GYRO_FS_SEL	Gyroscope FSR Value
000	±2000dps
001	±1000dps
010	±500dps
011	±250dps
100	±125dps
101	±62.5dps
110	±31.25dps
111	±15.625dps

Accelerometer ODR can be selected by programming the parameter ACCEL_ODR in bank 0, register 0x50h, bits 3:0 as shown below.

ACCEL_ODR	Accelerometer ODR Value
0000	Reserved
0001	Reserved
0010	Reserved
0011	8kHz
0100	4kHz
0101	2kHz
0110	1kHz
0111	200Hz (default)
1000	100Hz
1001	50Hz
1010	25Hz
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

Accelerometer FSR can be selected by programming the parameter ACCEL_FS_SEL in bank 0, register 0x50h, bits 7:5 as shown below.

ACCEL_FS_SEL	Accelerometer FSR Value
000	±16g
001	±8g
010	±4g

011	±2g
100	Reserved
101	Reserved
110	Reserved
111	Reserved

6 FIFO

The ICM-40605 contains a 1024 byte FIFO register that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO.

6.1 PACKET STRUCTURE

The following figure shows the FIFO packet structure supported in ICM-40605. Total packet size is 16 bytes. An additional special packet is available for keeping track of dropped packets during a FIFO overflow event.

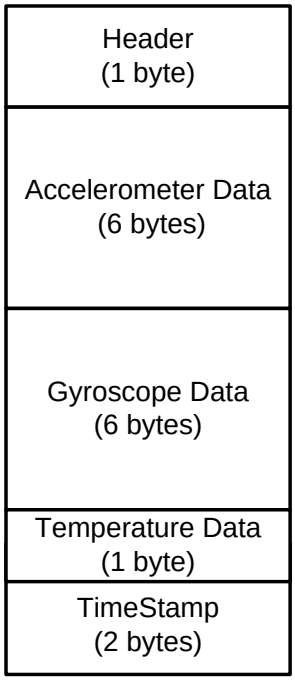

Figure 9. FIFO Packet Structure

6.2 FIFO HEADER

The following table shows the structure of the 1 byte FIFO header.

Bit Field	Item	Description
7	HEADER_MSG	1: FIFO is empty 0: Packet contains sensor data
6	HEADER_ACCEL	1: Packet has a new and valid sample of accel data, FIFO_ACCEL_EN must be 1 0: Packet does not contain a new and valid accel sample
5	HEADER_GYRO	1: Packet has a new and valid sample of gyro data, FIFO_GYRO_EN must be 1 0: Packet does not contain a new and valid gyro sample
4	-	Reserved
3:2	HEADER_TIMESTAMP_FSYNC	00: Reserved 01: Reserved 10: Packet contains ODR Timestamp 11: Packet contains FSYNC time, and this packet is flagged as first ODR after FSYNC
1	HEADER_ODR_ACCEL	1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel

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0	HEADER_ODR_GYRO	1: The ODR for gyro is different for this gyro data packet compared to the previous accel packet 0: The ODR for gyro is the same as the previous packet with accel

Note at least HEADER_ACCEL or HEADER_GYRO must be set for a sensor data packet to be set.

6.3 MAXIMUM FIFO STORAGE

The maximum number of packets that can be stored in FIFO is a variable quantity depending on the use case. As shown in the figure below, the physical FIFO size is 1024 bytes. 16 of these bytes are reserved to prevent reading a packet during write operation. The remaining FIFO size available for packet storage is 1008 bytes. Additionally a read cache of 32 bytes is available.

When there is no serial interface read operation, the read cache is not available for storing packets. In that case the total storage available is 63 packets (1008 bytes).

When serial interface read operation happens, depending on the read operation, any of the 32 bytes in read cache may become available for storing packets. In that case the total storage available is 64 packets (1024 bytes) or 65 packets (1040 bytes).

FIFO full interrupt may also be triggered at 62 packets (992 bytes). This occurs when the FIFO is programmed to work in Streaming mode and an overflow condition is reached.

Due to the non-deterministic nature of system operation, driver memory allocation should always allocate the largest size of 65 packets (1040 bytes).

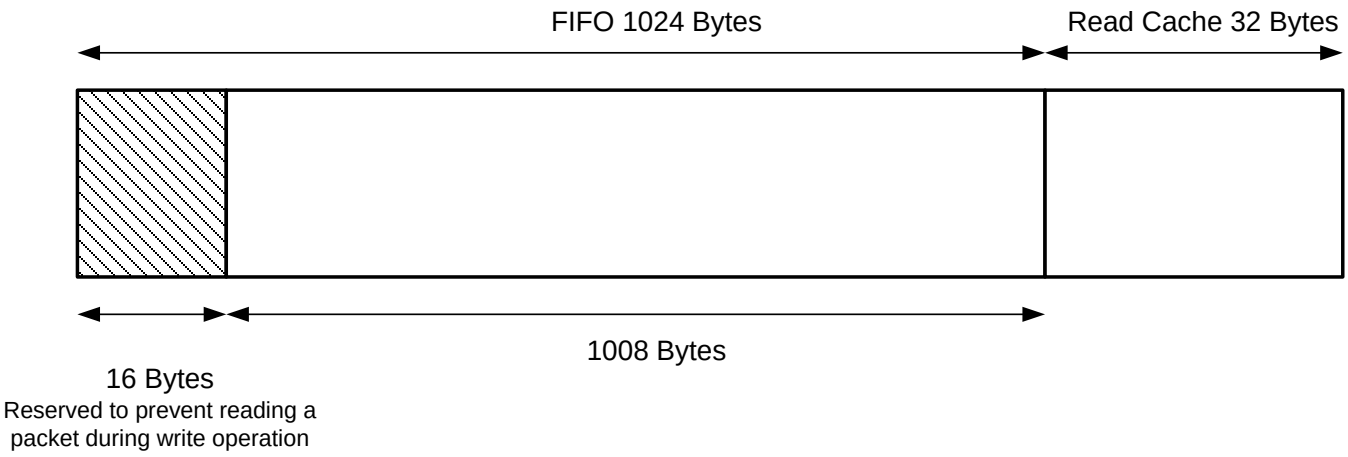

Figure 10. Maximum FIFO Storage

6.4 FIFO CONFIGURATION REGISTERS

The following control bits in bank 0, register 0x5Fh determine what data is placed into the FIFO. The values of these bits may change while the FIFO is being filled without corruption of the FIFO.

BIT	NAME	FUNCTION
3	FIFO_TMST_FSYNC_EN	Must be set to 1 for all use cases
2	FIFO_TEMP_EN	0: Default setting; Temperature sensor data not placed into FIFO 1: Enables temperature sensor data packet of 1-byte to be placed in FIFO
1	FIFO_GYRO_EN	0: Default setting; Gyroscope data not placed into FIFO 1: Enables gyroscope data packets of 6-bytes to be placed in FIFO
0	FIFO_ACCEL_EN	0: Default setting; Accelerometer data not placed into FIFO 1: Enables accelerometer data packets of 6-bytes to be placed in FIFO

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7 PROGRAMMABLE INTERRUPTS

The ICM-40605 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. The following configuration options are available for the interrupts

- Open drain or push-pull (INT1 is push-pull only, INT2 can be push-pull or open drain)
- Level or pulse mode
- Active high or active low

Any interrupt can be mapped to INT1 or INT2. Please refer to the register map for information on how to map various interrupts to INT1 or INT2.

8 DIGITAL INTERFACE

8.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-40605 can be accessed using either I²C at 1 MHz or SPI at 17 MHz. SPI operates in three-wire or four-wire mode. Pin assignments for serial interfaces are described in Section 4.1.

Note: To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the register field ui_sifs_cfg = `2b11. Setting this field should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 3.3.2.

8.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-40605 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 1 MHz.

The slave address of the ICM-40605 is b1101000, which is 7 bits long.

8.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

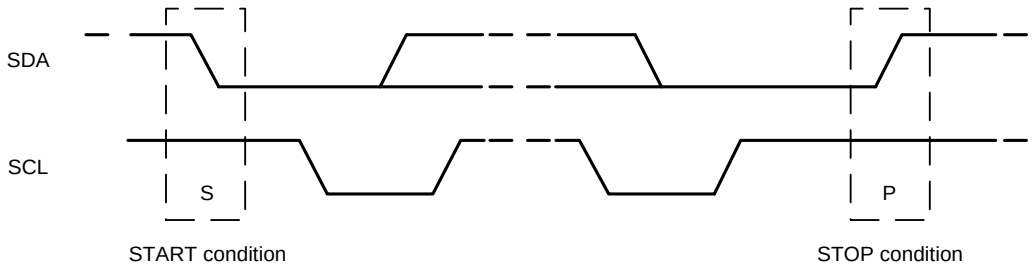

Figure 11. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

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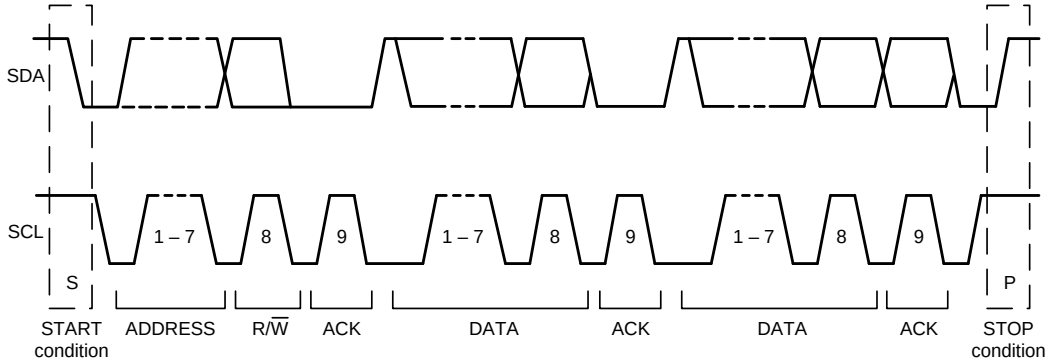

Figure 12. Complete I²C Data Transfer

To write the internal ICM-40605 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-40605 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-40605 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-40605 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-40605 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-40605, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-40605 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

8.4 I²C TERMS

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address

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W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-40605 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 12. I²C Terms

8.5 SPI INTERFACE

The ICM-40605 supports 3-wire and 4-wire SPI for the host interface. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line, and 4-wire SPI is a synchronous serial interface that uses two control lines and two data lines. The ICM-40605 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) for 4-wire SPI (or Serial Data IO (SDOI) for 3-wire SPI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (nCS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 17 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

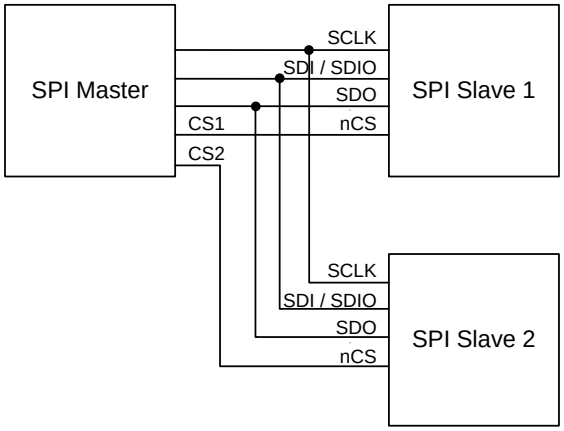

Figure 13. Typical SPI Master/Slave Configuration

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9 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

9.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

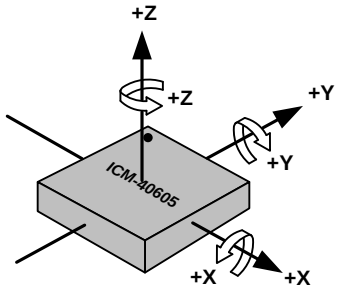

Figure 14. Orientation of Axes of Sensitivity and Polarity of Rotation

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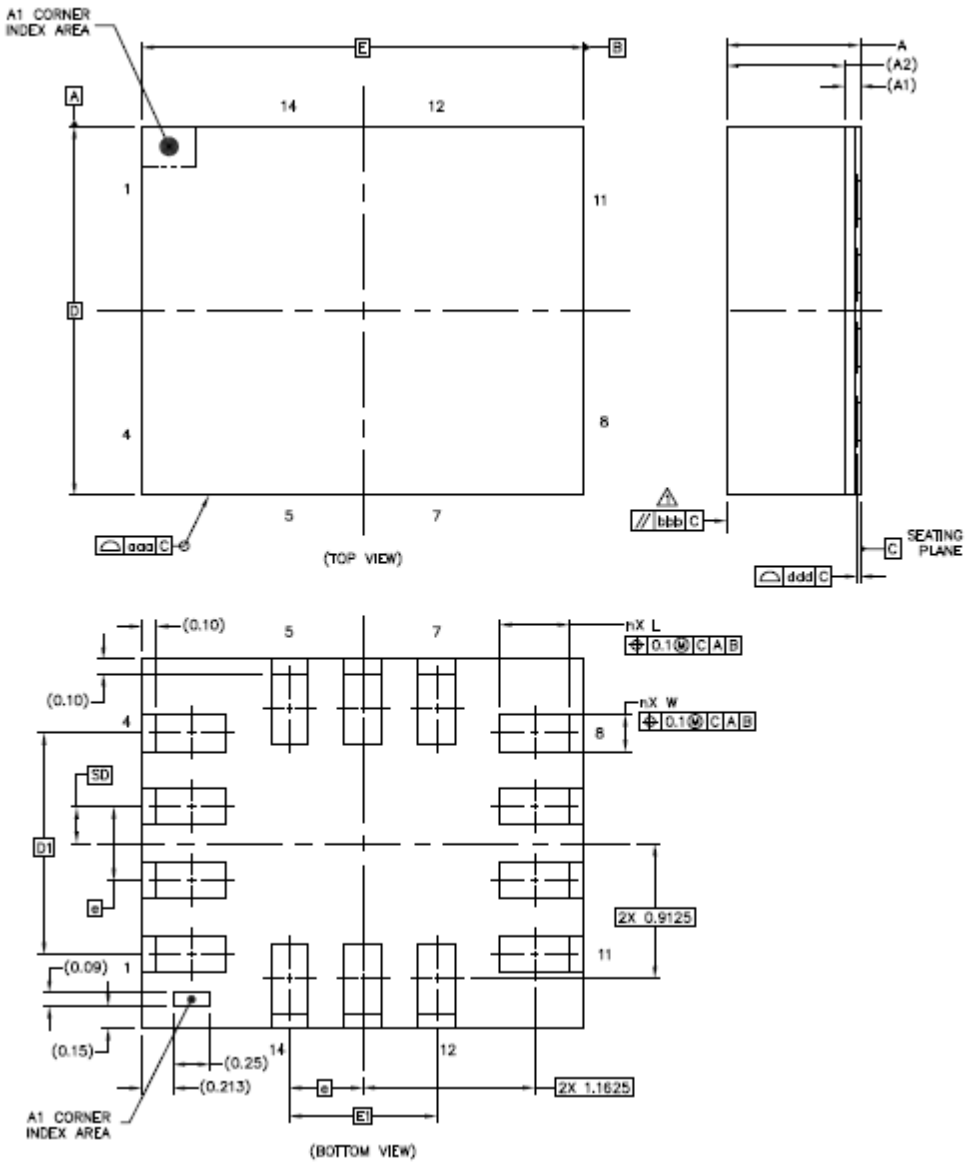
9.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.91) mm NiAu pad finish



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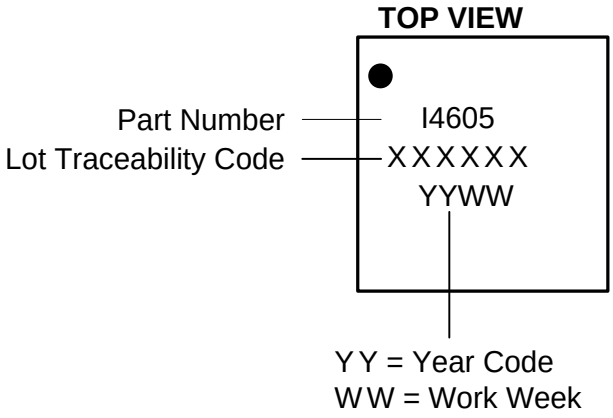
	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.85	0.91	0.97
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.8	REF
Body Size	D		2.5	BSC
	E		3	BSC
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.425	0.475	0.525
Lead Pitch	e		0.5	BSC
Lead Count	n		14	
Edge Pin Center to Center	D1		1.5	BSC
	E1		1	BSC
Body Center to Contact Pin	SD		0.25	BSC
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	

10 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-40605 devices is summarized below:

Part Number	Part Number Package Marking
ICM-40605	I4605



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11 USE NOTES

11.1 SPI SPEED

Default device SPI speed is 5MHz MAX. To support SPI speed at 17MHz MAX, SPI_SPEED_CONFIG value in register SPI_SPEED (register 0x13h, register-field 2:0) should be changed from default value 011 to 101.

12 REGISTER MAP

This section lists the register map for the ICM-40605, for user banks 0, 1, 2.

12.1 USER BANK 0 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11	17	DEVICE_CONFIG	R/W	-			SPI_MODE				SOFT_RESET_CONFIG
13	19	SPI_SPEED	R/W	-					SPI_SPEED_CONFIG		
14	20	INT_CONFIG		-		INT2_MODE	INT2_DRIVE_CIRCUIT	INT2_POLARITY	INT1_MODE	-	INT1_POLARITY
16	22	FIFO_CONFIG	R/W	FIFO_MODE		-					
1D	29	TEMP_DATA1	SYNCR	TEMP_DATA[15:8]							
1E	30	TEMP_DATA0	SYNCR	TEMP_DATA[7:0]							
1F	31	ACCEL_DATA_X1	SYNCR	ACCEL_DATA_X[15:8]							
20	32	ACCEL_DATA_X0	SYNCR	ACCEL_DATA_X[7:0]							
21	33	ACCEL_DATA_Y1	SYNCR	ACCEL_DATA_Y[15:8]							
22	34	ACCEL_DATA_Y0	SYNCR	ACCEL_DATA_Y[7:0]							
23	35	ACCEL_DATA_Z1	SYNCR	ACCEL_DATA_Z[15:8]							
24	36	ACCEL_DATA_Z0	SYNCR	ACCEL_DATA_Z[7:0]							
25	37	GYRO_DATA_X1	SYNCR	GYRO _DATA_X[15:8]							
26	38	GYRO _DATA_X0	SYNCR	GYRO _DATA_X[7:0]							
27	39	GYRO _DATA_Y1	SYNCR	GYRO _DATA_Y[15:8]							
28	40	GYRO _DATA_Y0	SYNCR	GYRO _DATA_Y[7:0]							
29	41	GYRO _DATA_Z1	SYNCR	GYRO_DATA_Z[15:8]							
2A	42	GYRO _DATA_Z0	SYNCR	GYRO_DATA_Z[7:0]							
2B	43	TMST_FSYNCL	SYNCR	TMST_FSYNC_DATA[7:0]							
2C	44	TMST_FSYNCH	SYNCR	TMST_FSYNC_DATA[15:8]							
2D	45	INT_STATUS	R/C	-	FSYNC_INT	PLL_RDY_INT	RESET_DONE_INT	DATA_RDY_INT	FIFO_THS_INT	FIFO_FULL_INT	AGC_RDY_INT
2E	46	FIFO_COUNTL	R	FIFO_COUNT[7:0]							
2F	47	FIFO_COUNTH	R	FIFO_COUNT[15:8]							
30	48	FIFO_DATA	R	FIFO_DATA							
4B	75	SIGNAL_PATH_RESET	W/C	-					TMST_STROBE	FIFO_FLUSH	-
4C	76	INTF_CONFIG0	R/W	-	FIFO_COUNT_REC	FIFO_COUNT_ENDIAN	SENSOR_DATA_ENDIAN	-		UI_SIFS_CFG	
4E	78	PWR_MGMT0	R/W	-		TEMP_DIS	IDLE	GYRO_MODE		ACCEL_MODE	
4F	79	GYRO_CONFIG0	R/W	GYRO_FS_SEL			-	GYRO_ODR			
50	80	ACCEL_CONFIG0	R/W	ACCEL_FS_SEL			-	ACCEL_ODR			
51	81	GYRO_CONFIG1	R/W	TEMP_FILT_BW			-	GYRO_UI_FILT_ORD		-	
52	82	GYRO_ACCEL_CONFIG0	R/W	ACCEL_UI_FILT_BW				GYRO_UI_FILT_BW			
53	83	ACCEL_CONFIG1	R/W	-			ACCEL_UI_FILT_ORD		-		
54	84	ACCEL_WOM_X_THR	R/W	WOM_X_TH							
55	85	ACCEL_WOM_Y_THR	R/W	WOM_Y_TH							
56	86	ACCEL_WOM_Z_THR	R/W	WOM_Z_TH							
57	87	SMD_CONFIG	R/W	-				WOM_INT_MODE	WOM_MODE	SMD_MODE	
59	89	INT_STATUS2	R/C	-				SMD_INT	WOM_Z_INT	WOM_Y_INT	WOM_X_INT
5A	90	TMST_CONFIG	R/W	-				TMST_RES	TMST_DELTA_EN	TMST_FSYNC_EN	TMST_EN
5F	95	FIFO_CONFIG1	R/W	-				FIFO_TMST_FSYNC_EN	FIFO_TEMP_EN	FIFO_GYRO_EN	FIFO_ACCEL_EN
60	96	FIFO_CONFIG2	R/W	FIFO_WM[7:0]							
61	97	FIFO_CONFIG3	R/W	FIFO_WM[15:8]							

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Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
62	98	FSYNC_CONFIG	R/W	-	FSYNC_UI_SEL			-		FSYNC_FLAG_CLEAR_SEL	FSYNC_POLARITY
63	99	INT_CONFIG0	R/W	-		DRDY_INT_CLEAR		FIFO_THS_INT_CLEAR		FIFO_FULL_INT_CLEAR	
65	101	INT_SOURCE0	R/W	-	FSYNC_INT1_EN	PLL_RDY_INT1_EN	RESET_DONE_INT1_EN	DRDY_INT1_EN	FIFO_THS_INT1_EN	FIFO_FULL_INT1_EN	AGC_RDY_INT1_EN
66	102	INT_SOURCE1	R/W	-				SMD_INT1_EN	WOM_Z_INT1_EN	WOM_Y_INT1_EN	WOM_X_INT1_EN
68	104	INT_SOURCE3	R/W	-	FSYNC_INT2_EN	PLL_RDY_INT2_EN	RESET_DONE_INT2_EN	DRDY_INT2_EN	FIFO_THS_INT2_EN	FIFO_FULL_INT2_EN	AGC_RDY_INT2_EN
69	105	INT_SOURCE4	R/W	-				SMD_INT2_EN	WOM_Z_INT2_EN	WOM_Y_INT2_EN	WOM_X_INT2_EN
6C	108	FIFO_LOST_PKT0	R	FIFO_LOST_PKT_CNT[7:0]							
6D	109	FIFO_LOST_PKT1	R	FIFO_LOST_PKT_CNT[15:8]							
70	112	SELF_TEST_CONFIG	R/W	-		EN_AZ_ST	EN_AY_ST	EN_AX_ST	EN_GZ_ST	EN_GY_ST	EN_GX_ST
75	117	WHO_AM_I	R	WHOAMI							
76	118	REG_BANK_SEL	R/W	-					BANK_SEL		
77	119	OFFSET_USER0	R/W	GYRO_X_OFFUSER[7:0]							
78	120	OFFSET_USER1	R/W	GYRO_Y_OFFUSER[11:8]				GYRO_X_OFFUSER[11:8]			
79	121	OFFSET_USER2	R/W	GYRO_Y_OFFUSER[7:0]							
7A	122	OFFSET_USER3	R/W	GYRO_Z_OFFUSER[7:0]							
7B	123	OFFSET_USER4	R/W	ACCEL_X_OFFUSER[11:8]				GYRO_Z_OFFUSER[11:8]			
7C	124	OFFSET_USER5	R/W	ACCEL_X_OFFUSER[7:0]							
7D	125	OFFSET_USER6	R/W	ACCEL_Y_OFFUSER[7:0]							
7E	126	OFFSET_USER7	R/W	ACCEL_Z_OFFUSER[11:8]				ACCEL_Y_OFFUSER[11:8]			
7F	127	OFFSET_USER8	R/W	ACCEL_Z_OFFUSER[7:0]							

12.2 USER BANK 1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0B	11	GYRO_CONFIG_STATIC2	R/W	-						GYRO_AAF_DIS	GYRO_NF_DIS
0C	12	GYRO_CONFIG_STATIC3	R/W	-		GYRO_AAF_DELT					
0D	13	GYRO_CONFIG_STATIC4	R/W	GYRO_AAF_DELTSQR[7:0]							
0E	14	GYRO_CONFIG_STATIC5	R/W	GYRO_AAF_BITSHIFT				GYRO_AAF_DELTSQR[11:8]			
0F	15	GYRO_CONFIG_STATIC6	R/W	GYRO_X_NF_COSWZ[7:0]							
10	16	GYRO_CONFIG_STATIC7	R/W	GYRO_Y_NF_COSWZ[7:0]							
11	17	GYRO_CONFIG_STATIC8	R/W	GYRO_Z_NF_COSWZ[7:0]							
12	18	GYRO_CONFIG_STATIC9	R/W	-		GYRO_Z_NF_COSWZ_SEL[0]	GYRO_Y_NF_COSWZ_SEL[0]	GYRO_X_NF_COSWZ_SEL[0]	GYRO_Z_NF_COSWZ[8]	GYRO_Y_NF_COSWZ[8]	GYRO_X_NF_COSWZ[8]
13	19	GYRO_CONFIG_STATIC10	R/W	-	GYRO_NF_BW_SEL			-			
5F	95	XG_ST_DATA	R/W	XG_ST_DATA							
60	96	YG_ST_DATA	R/W	YG_ST_DATA							
61	97	ZG_ST_DATA	R/W	ZG_ST_DATA							
62	98	TMSTVAL0	R	TMST_VALUE[7:0]							
63	99	TMSTVAL1	R	TMST_VALUE[15:8]							
64	100	TMSTVAL2	R	-				TMST_VALUE[19:16]			
7A	122	INTF_CONFIG4	R/W	-						SPI_AP_4WIRE	-

12.3 USER BANK 2 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03	03	ACCEL_CONFIG_STATIC2	R/W	-	ACCEL_AAF_DELT						ACCEL_AAF_DIS

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Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04	ACCEL_CONFIG_STATIC3	R/W	ACCEL_AAF_DELTSQR[7:0]							
05	05	ACCEL_CONFIG_STATIC4	R/W	ACCEL_AAF_BITSHIFT				ACCEL_AAF_DELTSQR[15:8]			
3B	59	XA_ST_DATA	R/W	XA_ST_DATA							
3C	60	YA_ST_DATA	R/W	YA_ST_DATA							
3D	61	ZA_ST_DATA	R/W	ZA_ST_DATA							

The default device configuration supports Big Endian data format. Descriptions of data registers in this document are based on Big Endian format. User may change to Little Endian data format using register INTF_CONFIG0 (address 0x4Ch) in Bank 0.

13 USER BANK 0 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 0.

Note: The device powers up in sleep mode.

13.1 DEVICE_CONFIG

Name: DEVICE_CONFIG Address: 17 (11h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4:1	SPI_MODE	SPI mode selection 0000: Mode 0 and Mode 3 (default) 0001: Mode 1 and Mode 2 Rest of the values are reserved
0	SOFT_RESET_CONFIG	Software reset configuration 0: Normal (default) 1: Enable reset

13.2 SPI_SPEED

Name: SPI_SPEED Address: 19 (13h) Serial IF: R/W Reset value: 0x03		
BIT	**NAME**	**FUNCTION**
7:3	-	Reserved
2:0	SPI_SPEED_CONFIG	011: 5MHz (default) 101: 17MHz Other values are reserved

Note: Default SPI speed is 5MHz. It may be changed to 17MHz by setting SPI_SPEED_CONFIG to 101.

13.3 INT_CONFIG

Name: INT_CONFIG Address: 20 (14h) Serial IF: R/W Reset value: 0x09		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5	INT2_MODE	INT2 interrupt mode 0: Pulsed mode 1: Latched mode
4	INT2_DRIVE_CIRCUIT	INT2 drive circuit 0: Open drain 1: Push pull
3	INT2_POLARITY	INT2 interrupt polarity 0: Active low

		1: Active high (default)
2	INT1_MODE	INT1 interrupt mode 0: Pulsed mode 1: Latched mode
1	-	Reserved
0	INT1_POLARITY	INT1 interrupt polarity 0: Active low 1: Active high (default)

13.4 FIFO_CONFIG

Name: FIFO_CONFIG
Address: 22 (16h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	FIFO_MODE	00: Bypass Mode (default) 01: Stream-to-FIFO Mode 10: STOP-on-FULL Mode 11: STOP-on-FULL Mode
5:0	-	Reserved

13.5 TEMP_DATA1

Name: TEMP_DATA1
Address: 29 (1Dh)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_DATA[15:8]	Upper byte of temperature data

13.6 TEMP_DATA0

Name: TEMP_DATA0
Address: 30 (1Eh)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_DATA[7:0]	Lower byte of temperature data

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 115.49) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA * 128 / 115.49) + 25

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13.7 ACCEL_DATA_X1

Name: ACCEL_DATA_X1
Address: 31 (1Fh)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X[15:8]	Upper byte of Accel X-axis data

13.8 ACCEL_DATA_X0

Name: ACCEL_DATA_X0
Address: 32 (20h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X[7:0]	Lower byte of Accel X-axis data

13.9 ACCEL_DATA_Y1

Name: ACCEL_DATA_Y1
Address: 33 (21h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[15:8]	Upper byte of Accel Y-axis data

13.10 ACCEL_DATA_Y0

Name: ACCEL_DATA_Y0
Address: 34 (22h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[7:0]	Lower byte of Accel Y-axis data

13.11 ACCEL_DATA_Z1

Name: ACCEL_DATA_Z1
Address: 35 (23h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[15:8]	Upper byte of Accel Z-axis data

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13.12 ACCEL_DATA_Z0

Name: ACCEL_DATA_Z0 Address: 36 (24h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_DATA_Z[7:0]	Lower byte of Accel Z-axis data

13.13 GYRO_DATA_X1

Name: GYRO_DATA_X1 Address: 37 (25h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_X[15:8]	Upper byte of Gyro X-axis data

13.14 GYRO_DATA_X0

Name: GYRO_DATA_X0 Address: 38 (26h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_X[7:0]	Lower byte of Gyro X-axis data

13.15 GYRO_DATA_Y1

Name: GYRO_DATA_Y1 Address: 39 (27h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Y[15:8]	Upper byte of Gyro Y-axis data

13.16 GYRO_DATA_Y0

Name: GYRO_DATA_Y0 Address: 40 (28h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Y[7:0]	Lower byte of Gyro Y-axis data

13.17 GYRO_DATA_Z1

Name: GYRO_DATA_Z1 Address: 41 (29h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Z[15:8]	Upper byte of Gyro Z-axis data

13.18 GYRO_DATA_Z0

Name: GYRO_DATA_Z0 Address: 42 (2Ah) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Z[7:0]	Lower byte of Gyro Z-axis data

13.19 TMST_FSYNCL

Name: TMST_FSYNCL Address: 43 (2Bh) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	tmst_fsync_data[7:0]	Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

13.20 TMST_FSYNCH

Name: TMST_FSYNCH Address: 44 (2Ch) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	tmst_fsync_data[15:8]	Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

13.21 INT_STATUS

Name: INT_STATUS Address: 45 (2Dh) Serial IF: R/C Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6	FSYNC_INT	This bit automatically sets to 1 when an FSYNC interrupt is generated. The bit clears to 0 after the register has been read.
5	PLL_RDY_INT	This bit automatically sets to 1 when a PLL Ready interrupt is generated. The bit clears to 0 after the register has been read.
4	RESET_DONE_INT	This bit automatically sets to 1 when a RESET DONE interrupt is generated. The bit clears to 0 after the register has been read.

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3	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.
2	FIFO_THS_INT	This bit automatically sets to 1 when the FIFO buffer reaches the threshold value. The bit clears to 0 after the register has been read.
1	FIFO_FULL_INT	This bit automatically sets to 1 when the FIFO buffer is full. The bit clears to 0 after the register has been read.
0	AGC_RDY_INT	This bit automatically sets to 1 when an AGC Ready interrupt is generated. The bit clears to 0 after the register has been read.

13.22 FIFO_COUNTL

Name: FIFO_COUNTL Address: 46 (2Eh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_COUNT[7:0]	Low Byte, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

13.23 FIFO_COUNTH

Name: FIFO_COUNTH Address: 47 (2Fh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_COUNT[15:8]	High Byte, count indicates the number of written bytes in the FIFO. Note: Must read FIFO_COUNTL to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

13.24 FIFO_DATA

Name: FIFO_DATA Address: 48 (30h) Serial IF: R Reset value: 0xFF		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_DATA	FIFO data port

13.25 SIGNAL_PATH_RESET

Name: SIGNAL_PATH_RESET Address: 75 (4Bh) Serial IF: W/C Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:3	-	Reserved
2	TMST_STROBE	When this bit is set to 1, the time stamp counter is latched into the time stamp register. This is a write on clear bit.

1	FIFO_FLUSH	When set to 1, FIFO will get flushed. FIFO flush requires special sequence of programming the registers. Please see use notes for details.
0	-	Reserved

13.26 INTF_CONFIG0

Name: INTF_CONFIG0
Address: 76 (4Ch)
Serial IF: R/W
Reset value: 0x30

BIT	NAME	FUNCTION
7	-	Reserved
6	FIFO_COUNT_REC	0: FIFO count is reported in bytes 1: FIFO count is reported in records (1 record = 16 bytes for gyro+accel+temp sensor data)
5	FIFO_COUNT_ENDIAN	0: FIFO count is reported in Little Endian format 1: FIFO count is reported in Big Endian format (default)
4	SENSOR_DATA_ENDIAN	0: Sensor data is reported in Little Endian format 1: Sensor data is reported in Big Endian format (default)
3:2	-	Reserved
1:0	UI_SIFS_CFG	10: Disable SPI 11: Disable I2C

13.27 PWR_MGMT0

Name: PWR_MGMT0
Address: 78 (4Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	TEMP_DIS	0: Temperature sensor is enabled (default) 1: Temperature sensor is disabled
4	IDLE	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state, since the RC oscillator will also be powered off
3:2	GYRO_MODE	00: Turns gyroscope off (default) 01: Places gyroscope in Standby Mode 10: Reserved 11: Places gyroscope in Low Noise (LN) Mode Gyroscope needs to be kept ON for a minimum of 80ms. When transitioning from OFF to any of the other modes, do not issue any register writes for 200µs.
1:0	ACCEL_MODE	00: Turns accelerometer off (default) 01: Turns accelerometer off 10: Reserved 11: Places accelerometer in Low Noise (LN) Mode When transitioning from OFF to any of the other modes, do not issue any register writes for 200µs.

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13.28 GYRO_CONFIG0

Name: GYRO_CONFIG0
Address: 79 (4Fh)
Serial IF: R/W
Reset value: 0x07

BIT	NAME	FUNCTION
7:5	GYRO_FS_SEL	Full scale select for gyroscope 000: ±2000dps (default) 001: ±1000dps 010: ±500dps 011: ±250dps 100: ±125dps 101: ±62.5dps 110: ±31.25dps 111: ±15.625dps
4	-	Reserved
3:0	GYRO_ODR	Gyroscope ODR selection 0000: Reserved 0001: Reserved 0010: Reserved 0011: 8kHz 0100: 4kHz 0101: 2kHz 0110: 1kHz 0111: 200Hz (default) 1000: 100Hz 1001: 50Hz 1010: 25Hz 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

13.29 ACCEL_CONFIG0

Name: ACCEL_CONFIG0
Address: 80 (50h)
Serial IF: R/W
Reset value: 0x07

BIT	NAME	FUNCTION
7:5	ACCEL_FS_SEL	Full scale select for accelerometer 000: ±16g (default) 001: ±8g 010: ±4g 011: ±2g 100: Reserved 101: Reserved 110: Reserved 111: Reserved
4	-	Reserved
3:0	ACCEL_ODR	Accelerometer ODR selection 0000: Reserved

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		0001: Reserved 0010: Reserved 0011: 8kHz 0100: 4kHz 0101: 2kHz 0110: 1kHz 0111: 200Hz (default) 1000: 100Hz 1001: 50Hz 1010: 25Hz 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

13.30 GYRO_CONFIG1

Name: GYRO_CONFIG1
Address: 81 (51h)
Serial IF: R/W
Reset value: 0x1A

BIT	NAME	FUNCTION
7:5	TEMP_FILT_BW	Sets the bandwidth of the temperature signal DLPF 000: DLPF BW = 4000Hz; DLPF Latency = 0.125ms (default) 001: DLPF BW = 170Hz; DLPF Latency = 1ms 010: DLPF BW = 82Hz; DLPF Latency = 2ms 011: DLPF BW = 40Hz; DLPF Latency = 4ms 100: DLPF BW = 20Hz; DLPF Latency = 8ms 101: DLPF BW = 10Hz; DLPF Latency = 16ms 110: DLPF BW = 5Hz; DLPF Latency = 32ms 111: DLPF BW = 5Hz; DLPF Latency = 32ms
4	-	Reserved
3:2	GYRO_UI_FILT_ORD	Selects order of GYRO FIR filter 00: 1st Order 01: 2nd Order 10: 3rd Order 11: Reserved
1:0	-	Reserved

13.31 GYRO_ACCEL_CONFIG0

Name: GYRO_ACCEL_CONFIG0
Address: 82 (52h)
Serial IF: R/W
Reset value: 0x11

BIT	NAME	FUNCTION
7:4	ACCEL_UI_FILT_BW	Bandwidth for Accel LPF 0 BW=ODR/2 FIR 1 BW=max(400Hz, ODR)/4 (default) 2 BW=max(400Hz, ODR)/5 3 BW=max(400Hz, ODR)/8 4 BW=max(400Hz, ODR)/10

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		5 BW=max(400Hz, ODR)/16 6 BW=max(400Hz, ODR)/20 7 BW=max(400Hz, ODR)/40 8 to 15: Reserved
3:0	GYRO_UI_FILT_BW	Bandwidth for Gyro LPF 0 BW=ODR/2 FIR 1 BW=max(400Hz, ODR)/4 (default) 2 BW=max(400Hz, ODR)/5 3 BW=max(400Hz, ODR)/8 4 BW=max(400Hz, ODR)/10 5 BW=max(400Hz, ODR)/16 6 BW=max(400Hz, ODR)/20 7 BW=max(400Hz, ODR)/40 8 to 15: Reserved

13.32 ACCEL_CONFIG1

Name: ACCEL_CONFIG1
Address: 83 (53h)
Serial IF: R/W
Reset value: 0x15

BIT	NAME	FUNCTION
7:5	-	Reserved
4:3	ACCEL_UI_FILT_ORD	Selects order of ACCEL FIR filter 00: 1st Order 01: 2nd Order 10: 3rd Order 11: Reserved
2:0	-	Reserved

13.33 ACCEL_WOM_X_THR

Name: ACCEL_WOM_X_THR
Address: 84 (54h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_X_TH	Threshold value for the Wake on Motion Interrupt for X-axis accelerometer

13.34 ACCEL_WOM_Y_THR

Name: ACCEL_WOM_Y_THR
Address: 85 (55h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_Y_TH	Threshold value for the Wake on Motion Interrupt for Y-axis accelerometer

13.35 ACCEL_WOM_Z_THR

Name: ACCEL_WOM_Z_THR

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Address: 86 (56h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	WOM_Z_TH	Threshold value for the Wake on Motion Interrupt for Z-axis accelerometer

13.36 SMD_CONFIG

Name: SMD_CONFIG Address: 87 (57h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	WOM_INT_MODE	0: Set WoM interrupt on the OR of all enabled accelerometer thresholds 1: Set WoM interrupt on the AND of all enabled accelerometer threshold
2	WOM_MODE	0: Initial sample is stored, future samples are compared to initial sample 1: Compare current sample to previous sample
1:0	SMD_MODE	00: SMD disabled 01: Reserved 10: SMD short (1 sec wait): An SMD event is detected when two WOM are detected 1 sec apart 11: SMD long (3 sec wait): An SMD event is detected when two WOM are detected 3 sec apart

13.37 INT_STATUS2

Name: INT_STATUS2 Address: 89 (59h) Serial IF: R/C Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	SMD_INT	SMD interrupt status, clears on read
2	WOM_Z_INT	Z-axis accelerometer WoM interrupt status, clears on read
1	WOM_Y_INT	Y-axis accelerometer WoM interrupt status, clears on read
0	WOM_X_INT	X-axis accelerometer WoM interrupt status, clears on read

13.38 TMST_CONFIG

Name: TMST_CONFIG Address: 90 (5Ah) Serial IF: R/W Reset value: 0x23		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	TMST_RES	Time Stamp resolution: When set to 0 (default), time stamp resolution is 1 µs. When set to 1, resolution is 16µs
2	TMST_DELTA_EN	Time Stamp delta enable: When set to 1, the time stamp field contains the measurement of time since the last occurrence of ODR.
1	TMST_FSYNC_EN	Time Stamp register FSYNC enable (default). When set to 1, the contents of the Timestamp feature of FSYNC is enabled. The user also needs to select

		FIFO_TMST_FSYNC_EN in order to propagate the timestamp value to the FIFO.
0	TMST_EN	0: Time Stamp register disable 1: Time Stamp register enable (default)

13.39 FIFO_CONFIG1

Name: FIFO_CONFIG1
Address: 95 (5Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3	FIFO_TMST_FSYNC_EN	Must be set to 1 for all use cases
2	FIFO_TEMP_EN	Must be set to 1 for all use cases
1	FIFO_GYRO_EN	Must be set to 1 for all use cases
0	FIFO_ACCEL_EN	Must be set to 1 for all use cases

13.40 FIFO_CONFIG2

Name: FIFO_CONFIG2
Address: 96 (60h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_WM[7:0]	Lower byte of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes. FIFO_THS_INT1_EN and FIFO_THS_INT2_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source.

13.41 FIFO_CONFIG3

Name: FIFO_CONFIG3
Address: 97 (61h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_WM[15:8]	Upper byte of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes. FIFO_THS_INT1_EN and FIFO_THS_INT2_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source.

Note: Do not set FIFO_WM to value 0.

13.42 FSYNC_CONFIG

Name: FSYNC_CONFIG
Address: 98 (62h)
Serial IF: R/W
Reset value: 0x10

BIT	NAME	FUNCTION

7	-	Reserved
6:4	FSYNC_UI_SEL	000: Do not tag FSYNC flag 001: Tag FSYNC flag to TEMP_OUT LSB 010: Tag FSYNC flag to GYRO_XOUT LSB 011: Tag FSYNC flag to GYRO_YOUT LSB 100: Tag FSYNC flag to GYRO_ZOUT LSB 101: Tag FSYNC flag to ACCEL_XOUT LSB 110: Tag FSYNC flag to ACCEL_YOUT LSB 111: Tag FSYNC flag to ACCEL_ZOUT LSB
3:2	-	Reserved
1	FSYNC_FLAG_CLEAR_SEL	0: FSYNC flag is cleared when sensor register is updated 1: FSYNC flag is cleared when UI interface reads the sensor register LSB of FSYNC tagged axis
0	FSYNC_POLARITY	0: Start from Rising edge of FSYNC pulse to measure FSYNC interval 1: Start from Falling edge of FSYNC pulse to measure FSYNC interval

13.43 INT_CONFIG0

Name: INT_CONFIG0
Address: 99 (63h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	DRDY_INT_CLEAR	Data Ready Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read
3:2	FIFO_THS_INT_CLEAR	FIFO Threshold Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read
1:0	FIFO_FULL_INT_CLEAR	FIFO Full Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read

13.44 INT_SOURCE0

Name: INT_SOURCE0
Address: 101 (65h)
Serial IF: R/W
Reset value: 0x10

BIT	NAME	FUNCTION
7	-	Reserved
6	FSYNC_INT1_EN	Enable FSYNC as interrupt source for INT1
5	PLL_RDY_INT1_EN	Enable PLL Ready as interrupt source for INT1
4	RESET_DONE_INT1_EN	Enable Reset Done as interrupt source for INT1
3	DRDY_INT1_EN	Enable Data Ready as interrupt source for INT1
2	FIFO_THS_INT1_EN	Enable FIFO Threshold as interrupt source for INT1

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1	FIFO_FULL_INT1_EN	Enable FIFO Full as interrupt source for INT1
0	AGC_RDY_INT1_EN	Enable AGC Ready as interrupt source for INT1

13.45 INT_SOURCE1

Name: INT_SOURCE1
Address: 102 (66h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3	SMD_INT1_EN	Enable SMD as interrupt source for INT1
2	WOM_Z_INT1_EN	Enable Z-axis WOM as interrupt source for INT1
1	WOM_Y_INT1_EN	Enable Y-axis WOM as interrupt source for INT1
0	WOM_X_INT1_EN	Enable X-axis WOM as interrupt source for INT1

13.46 INT_SOURCE3

Name: INT_SOURCE3
Address: 104 (68h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	FSYNC_INT2_EN	Enable FSYNC as interrupt source for INT2
5	PLL_RDY_INT2_EN	Enable PLL Ready as interrupt source for INT2
4	RESET_DONE_INT2_EN	Enable Reset Done as interrupt source for INT2
3	DRDY_INT2_EN	Enable Data Ready as interrupt source for INT2
2	FIFO_THS_INT2_EN	Enable FIFO Threshold as interrupt source for INT2
1	FIFO_FULL_INT2_EN	Enable FIFO Full as interrupt source for INT2
0	AGC_RDY_INT2_EN	Enable AGC Ready as interrupt source for INT2

13.47 INT_SOURCE4

Name: INT_SOURCE4
Address: 105 (69h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3	SMD_INT2_EN	Enable SMD as interrupt source for INT2
2	WOM_Z_INT2_EN	Enable Z-axis WOM as interrupt source for INT2
1	WOM_Y_INT2_EN	Enable Y-axis WOM as interrupt source for INT2
0	WOM_X_INT2_EN	Enable X-axis WOM as interrupt source for INT2

13.48 FIFO_LOST_PKT0

Name: FIFO_LOST_PKT0
Address: 108 (6Ch)

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Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_LOST_PKT_CNT[7:0]	Low byte, number of packets lost in the FIFO

13.49 FIFO_LOST_PKT1

Name: FIFO_LOST_PKT1 Address: 109 (6Dh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_LOST_PKT_CNT[15:8]	High byte, number of packets lost in the FIFO

13.50 SELF_TEST_CONFIG

Name: SELF_TEST_CONFIG Address: 112 (70h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5	EN_AZ_ST	Enable Z-accel self-test
4	EN_AY_ST	Enable Y-accel self-test
3	EN_AX_ST	Enable X-accel self-test
2	EN_GZ_ST	Enable Z-gyro self-test
1	EN_GY_ST	Enable Y-gyro self-test
0	EN_GX_ST	Enable X-gyro self-test

13.51 WHO_AM_I

Name: WHO_AM_I Address: 117 (75h) Serial IF: R Reset value: 0x33		
BIT	**NAME**	**FUNCTION**
7:0	WHOAMI	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x33. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor.

13.52 REG_BANK_SEL

Note: This register is accessible from register banks 0, 1, 2

Name: REG_BANK_SEL Address: 118 (76h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**

7:3	-	Reserved
2:0	BANK_SEL	Register bank selection 000: Bank 0 (default) 001: Bank 1 010: Bank 2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

13.53 OFFSET_USER0

Name: OFFSET_USER0
Address: 119 (77h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_X_OFFUSER[7:0]	Lower bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.54 OFFSET_USER1

Name: OFFSET_USER1
Address: 120 (78h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	GYRO_Y_OFFUSER[11:8]	Upper bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
3:0	GYRO_X_OFFUSER[11:8]	Upper bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.55 OFFSET_USER2

Name: OFFSET_USER2
Address: 121 (79h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Y_OFFUSER[7:0]	Lower bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.56 OFFSET_USER3

Name: OFFSET_USER3
Address: 122 (7Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION

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7:0	GYRO_Z_OFFUSER[7:0]	Lower bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.57 OFFSET_USER4

Name: OFFSET_USER4
Address: 123 (7Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	ACCEL_X_OFFUSER[11:8]	Upper bits of X-accel offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
3:0	GYRO_Z_OFFUSER[11:8]	Upper bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.58 OFFSET_USER5

Name: OFFSET_USER5
Address: 124 (7Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_X_OFFUSER[7:0]	Lower bits of X-accel offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.59 OFFSET_USER6

Name: OFFSET_USER6
Address: 125 (7Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Y_OFFUSER[7:0]	Lower bits of Y-accel offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.60 OFFSET_USER7

Name: OFFSET_USER7
Address: 126 (7Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	ACCEL_Z_OFFUSER[11:8]	Upper bits of Z-accel offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
3:0	ACCEL_Y_OFFUSER[11:8]	Upper bits of Y-accel offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

13.61 OFFSET_USER8

Name: OFFSET_USER8 Address: 127 (7Fh) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_Z_OFFUSER[7:0]	Lower bits of Z-accel offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

14 USER BANK 1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 1.

14.1 GYRO_CONFIG_STATIC2

Name: GYRO_CONFIG_STATIC2
Address: 11 (0Bh)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:2	-	Reserved
1	GYRO_AAF_DIS	0: Enable gyroscope anti-aliasing filter 1: Disable gyroscope anti-aliasing filter (default)
0	GYRO_NF_DIS	0: Enable gyroscope notch filter 1: Disable gyroscope notch filter (default)

14.2 GYRO_CONFIG_STATIC3

Name: GYRO_CONFIG_STATIC3
Address: 12 (0Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	GYRO_AAF_DELT	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

14.3 GYRO_CONFIG_STATIC4

Name: GYRO_CONFIG_STATIC4
Address: 13 (0Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_AAF_DELTSQR [7:0]	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

14.4 GYRO_CONFIG_STATIC5

Name: GYRO_CONFIG_STATIC5
Address: 14 (0Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	GYRO_AAF_BITSHIFT	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details
3:0	GYRO_AAF_DELTSQR [11:8]	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

14.5 GYRO_CONFIG_STATIC6

Name: GYRO_CONFIG_STATIC6 Address: 15 (0Fh) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_X_NF_COSWZ[7:0]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details

14.6 GYRO_CONFIG_STATIC7

Name: GYRO_CONFIG_STATIC7 Address: 16 (10h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_Y_NF_COSWZ[7:0]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details

14.7 GYRO_CONFIG_STATIC8

Name: GYRO_CONFIG_STATIC8 Address: 17 (11h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_Z_NF_COSWZ[7:0]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details

14.8 GYRO_CONFIG_STATIC9

Name: GYRO_CONFIG_STATIC9 Address: 18 (12h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5	GYRO_Z_NF_COSWZ_SEL	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details
4	GYRO_Y_NF_COSWZ_SEL	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details
3	GYRO_X_NF_COSWZ_SEL	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details
2	GYRO_Z_NF_COSWZ[8]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details
1	GYRO_Y_NF_COSWZ[8]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details
0	GYRO_X_NF_COSWZ[8]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details

14.9 GYRO_CONFIG_STATIC10

Name: GYRO_CONFIG_STATIC10
Address: 19 (13h)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7	-	Reserved
6:4	GYRO_NF_BW_SEL	Selects bandwidth for gyroscope notch filter See section 5.1 for details
3:0	-	Reserved

14.10 XG_ST_DATA

Name: XG_ST_DATA
Address: 95 (5Fh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)

BIT	NAME	FUNCTION
7:0	XG_ST_DATA	X-gyro self-test data

14.11 YG_ST_DATA

Name: YG_ST_DATA
Address: 96 (60h)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)

BIT	NAME	FUNCTION
7:0	YG_ST_DATA	Y-gyro self-test data

14.12 ZG_ST_DATA

Name: ZG_ST_DATA
Address: 97 (61h)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)

BIT	NAME	FUNCTION
7:0	ZG_ST_DATA	Z-gyro self-test data

14.13 TMSTVAL0

Name: TMSTVAL0
Address: 98 (62h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TMST_VALUE[7:0]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

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14.14 TMSTVAL1

Name: TMSTVAL1 Address: 99 (63h) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	TMST_VALUE[15:8]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

14.15 TMSTVAL2

Name: TMSTVAL2 Address: 100 (64h) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3:0	TMST_VALUE[19:16]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

14.16 INTF_CONFIG4

Name: INTF_CONFIG4 Address: 122 (7Ah) Serial IF: R/W Reset value: 0x02		
BIT	**NAME**	**FUNCTION**
7:2	-	Reserved
1	SPI_AP_4WIRE	0: AP interface uses 3-wire SPI mode 1: AP interface uses 4-wire SPI mode (default)
0	-	Reserved

15 USER BANK 2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 2.

15.1 ACCEL_CONFIG_STATIC2

Name: ACCEL_CONFIG_STATIC2
Address: 03 (03h)
Serial IF: R/W
Reset value: 0x7F

BIT	NAME	FUNCTION
7	-	Reserved
6:1	ACCEL_AAF_DELT	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details
0	ACCEL_AAF_DIS	0: Enable accelerometer anti-aliasing filter 1: Disable accelerometer anti-aliasing filter (default)

15.2 ACCEL_CONFIG_STATIC3

Name: ACCEL_CONFIG_STATIC3
Address: 04 (04h)
Serial IF: R/W
Reset value: 0x81

BIT	NAME	FUNCTION
7:0	ACCEL_AAF_DELTSQR[7:0]	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details

15.3 ACCEL_CONFIG_STATIC4

Name: ACCEL_CONFIG_STATIC4
Address: 05 (05h)
Serial IF: R/W
Reset value: 0x3F

BIT	NAME	FUNCTION
7:4	ACCEL_AAF_BITSHIFT	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details
3:0	ACCEL_AAF_DELTSQR[11:8]	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details

15.4 XA_ST_DATA

Name: XA_ST_DATA
Address: 59 (3Bh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)

BIT	NAME	FUNCTION
7:0	XA_ST_DATA	X-accel self-test data

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15.5 YA_ST_DATA

Name: YA_ST_DATA Address: 60 (3Ch) Serial IF: R/W Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)		
BIT	**NAME**	**FUNCTION**
7:0	YA_ST_DATA	Y-accel self-test data

15.6 ZA_ST_DATA

Name: ZA_ST_DATA Address: 61 (3Dh) Serial IF: R/W Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)		
BIT	**NAME**	**FUNCTION**
7:0	ZA_ST_DATA	Z-accel self-test data

16 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

17 DOCUMENT INFORMATION

17.1 REVISION HISTORY

Revision Date	Revision	Description
03/07/2017	0.1	Initial Release
05/10/2017	0.2	Updated Sections 3, 4, 9, 10, 11
07/12/2017	0.3	Updated Sections 3, 5, 6, 12, 13
08/11/2017	0.4	Updated Sections 3, 4, 12, 13
08/22/2017	0.5	Updated Section 4
08/28/2017	0.6	Updated Sections 3, 13
09/08/2017	0.7	Updated Sections 3, 13
11/09/2017	1.0	Updated Sections 2, 3, 4, 8, 12, 13